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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/604,646 | 08/06/2003 | Chien-Sheng Yang | ADTP0120USA | 1645 |

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| EXAMINER | |
|---|---|
| PATEL, NITIN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2673 | |

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/604,646 | YANG, CHIEN-SHENG | |
| | Examiner | Art Unit | |
| | Nitin Patel | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6 and 7* is/are rejected.

7)☒ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the common voltage drivers comprise polysilicon thin film transistors as claimed in claim 2 and also the common voltage drivers, the scan line driver, the data line driver and the timing control circuit comprise polysilicon thin film transistors in claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: In claim 2, the common voltage drivers comprise polysilicon thin film transistors. In claim 5, the common voltage drivers, the scan line driver, the data line driver and the timing control circuit comprise polysilicon thin film transistors.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,3,4,6,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebiguchi (U.S. Patent No. 6,225,967).

As per claim 1, Hebiguchi discloses a polysilicon thin film transistor liquid crystal display comprising: a panel (In col.5 lines 49-55); a plurality of display cells (In fig.8 display cells read as R, G, B); a plurality of scan lines formed in the panel and coupled to the display cells (In col.4 read as gate lines G1, G2... lines13-15); a plurality of data lines (In col.4 lines 10-13 read as source lines S1, S2...) formed in the panel and coupled to the display cells; and a plurality of common voltage drivers(In col.9 lines 17-21 common drivers CD1-CD3) formed in the panel.

Hebiguchi does not specifically shows a common voltage layer formed in the panel and common voltage applied to the common voltage layer. It would have been obvious to one of ordinary skill in the art, at the time of the invention was made that it is well known in the art, in liquid crystal display having substrates (In Col.9 lines 6-10) for sending data signals and scan signal to the pixels using drivers such as taught by Hebiguchi to have a common layer to send common voltages from the common voltage drivers (CD1-CD3) to pixels to change the state of the pixel to use purpose.

As per claim 3, Hebiguchi disclose the polysilicon thin film transistor liquid crystal display (In col.5 lines 49-54) wherein the common voltage is an alternating voltage (In col.9 lines 15-27).

As per claim 4, Hebiguchi also disclose the liquid crystal display (In fig.1 element 10) a scan line driver (GD1) coupled to the plurality of scan lines (In fig.1 lines G1..G3); at least a data line driver (SD1) coupled to the plurality of data lines (S1..S3); and a timing control circuit (as best understood by examiner a dot clock reading signals In col.6 lines 47-50 and In col.7 lines 64-67 to Col.8 lines 1-10) for generating a timing signal; wherein the scan line driver and the data line driver control operations of the display cells based on the timing signal.

As per claim 7, Hebiguchi disclose in each display cell (R, G, B cell)) further comprises: a liquid crystal component (element T in fig.2) comprising: a pixel electrode(R, G, B cell); and a common electrode (common drivers Cd1-Cd3 connected to the common electrode via a layer In col.4 lines 5-20) coupled to the common voltage layer; and a polysilicon thin film transistor (In col.5 lines 50-55) comprising: a gate

electrically (In fig.2 gate lines connected to Gd1) connected to a corresponding scan line; a source(source of the transistor T) electrically connected to a corresponding data line(lines S1); and a drain electrically connected to the pixel(drain of the transistor T is connected to R,G,B cells) electrode of the liquid crystal component.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hebiguchi (U.S. Patent No. 6,225,967) in view of Applicant's Admitted Prior Art (AAPA).

As per claim 6, Hebiguchi disclose a polysilicon thin film transistor liquid crystal display (In col.5 lines 49-54). Hebiguchi does not specifically teach an interface for receiving and transmitting an image signal such that the display cells operate based on the image signal.

AAPA discloses an interface (element 24 In fig.1 and see section 0006) for receiving and transmitting signals.

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to have incorporated the teaching of interface circuit of AAPA's with display device of Hebiguchi's because it would have received and send data to the related logic circuits such that corresponding images are displayed in the pixel region.

***Allowable Subject Matter***

6. Claims 2,5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to teach or suggest the polysilicon thin film transistor liquid crystal display, wherein the common voltage drivers comprise polysilicon thin film transistors as claimed in claim 2.

The prior art fails to teach or suggest the polysilicon thin film transistor liquid crystal display, wherein the common voltage drivers, the scan line driver, the data line driver, and the timing control circuit comprise polysilicon thin film transistors as claimed in claim 5.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP Nitin Patel

October 28, 2005